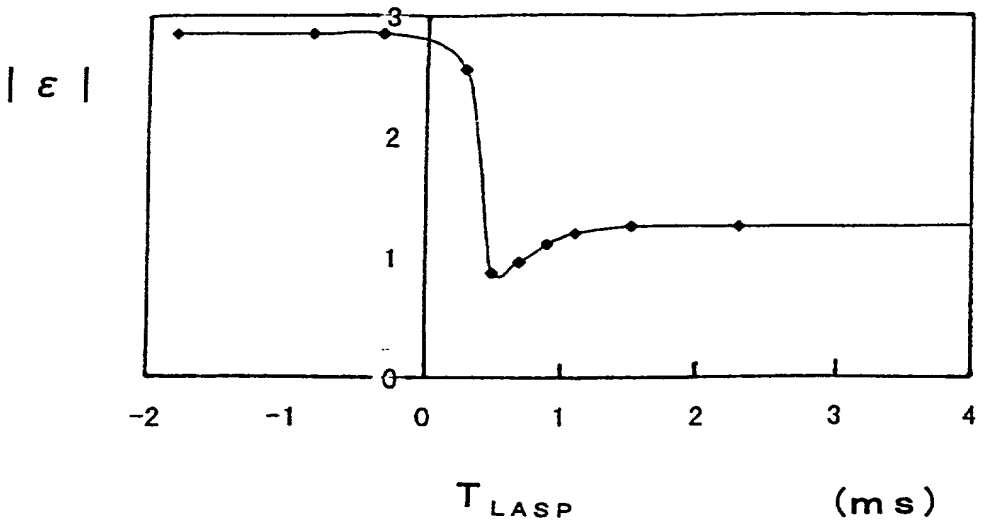
Fig. 1



* "0 ms" : At Power Off State

Fig. 2

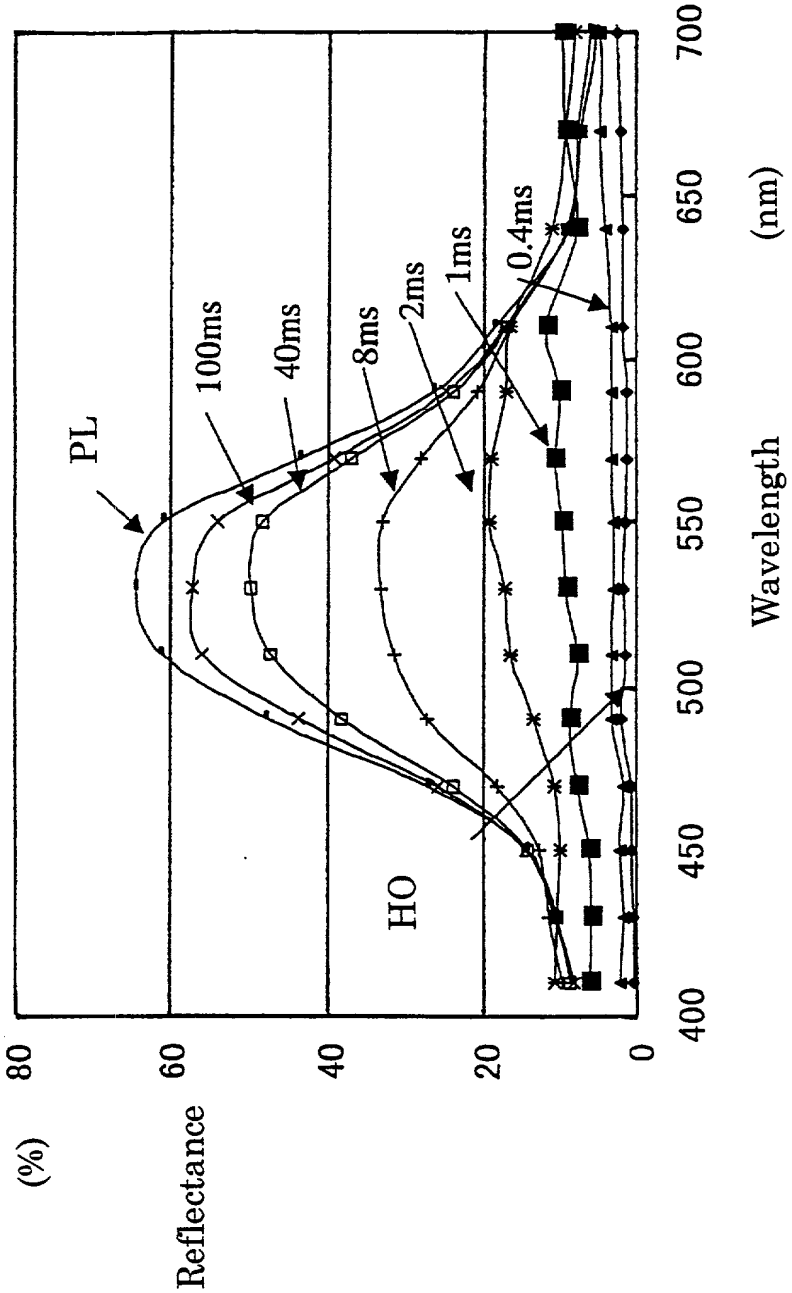

PL
100ms
40ms
8ms
2ms
1ms
0.4ms
HO
Reflectance
(%)
80
60
40
20
0
400
450
500
550
600
650
700
Wavelength
(nm)

Fig. 3

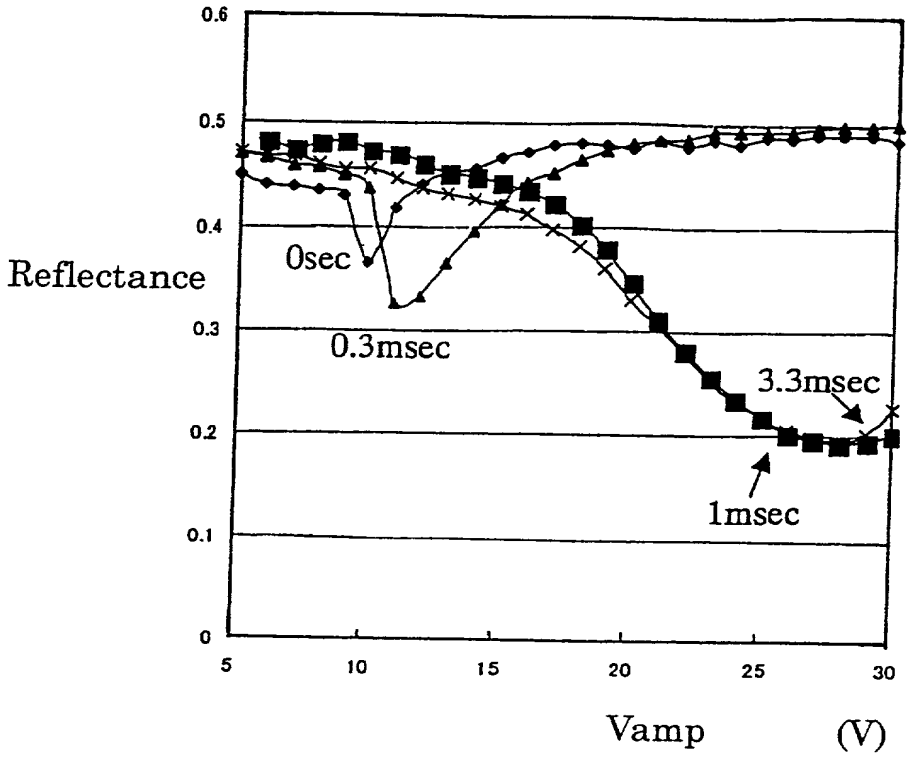

0.6
0.5
0.4
0.3
0.2
0.1
0
Reflectance
0sec
0.3msec
3.3msec
1msec
5
10
15
20
25
30
Vamp
(V)

Fig. 4

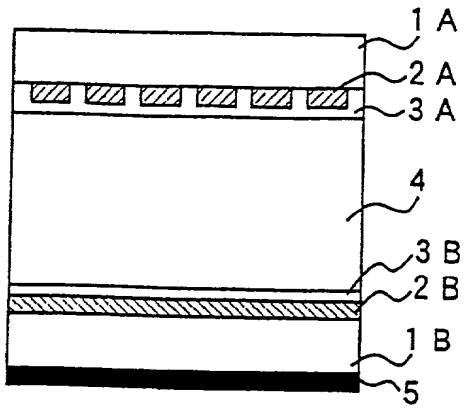

1 A
2 A
3 A
4
3 B
2 B
1 B
5

Fig. 5

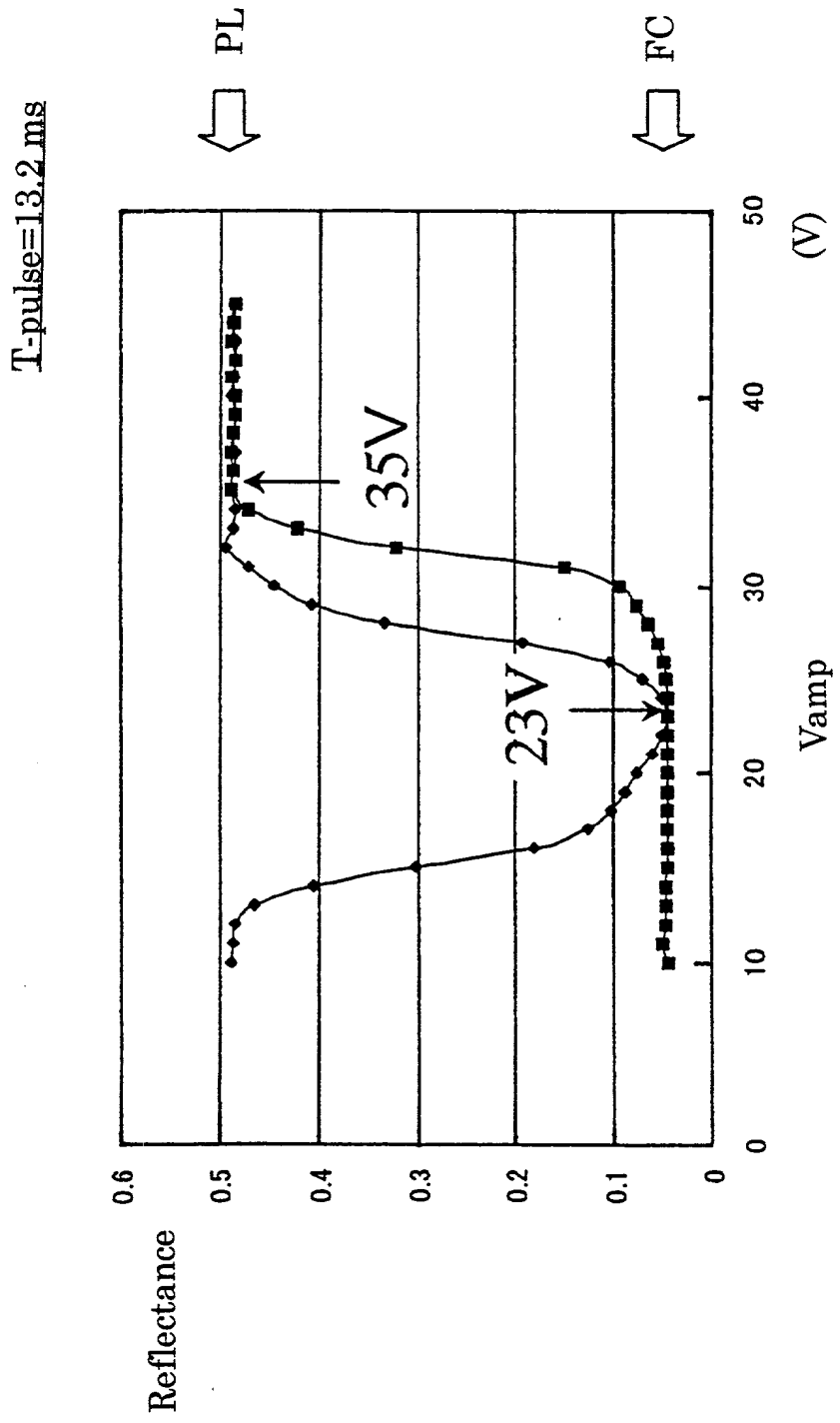

T-pulse=13.2 ms
PL
FC
35V
23V
Reflectance
0.6
0.5
0.4
0.3
0.2
0.1
0
Vamp
0
10
20
30
40
50
(V)

Fig. 6

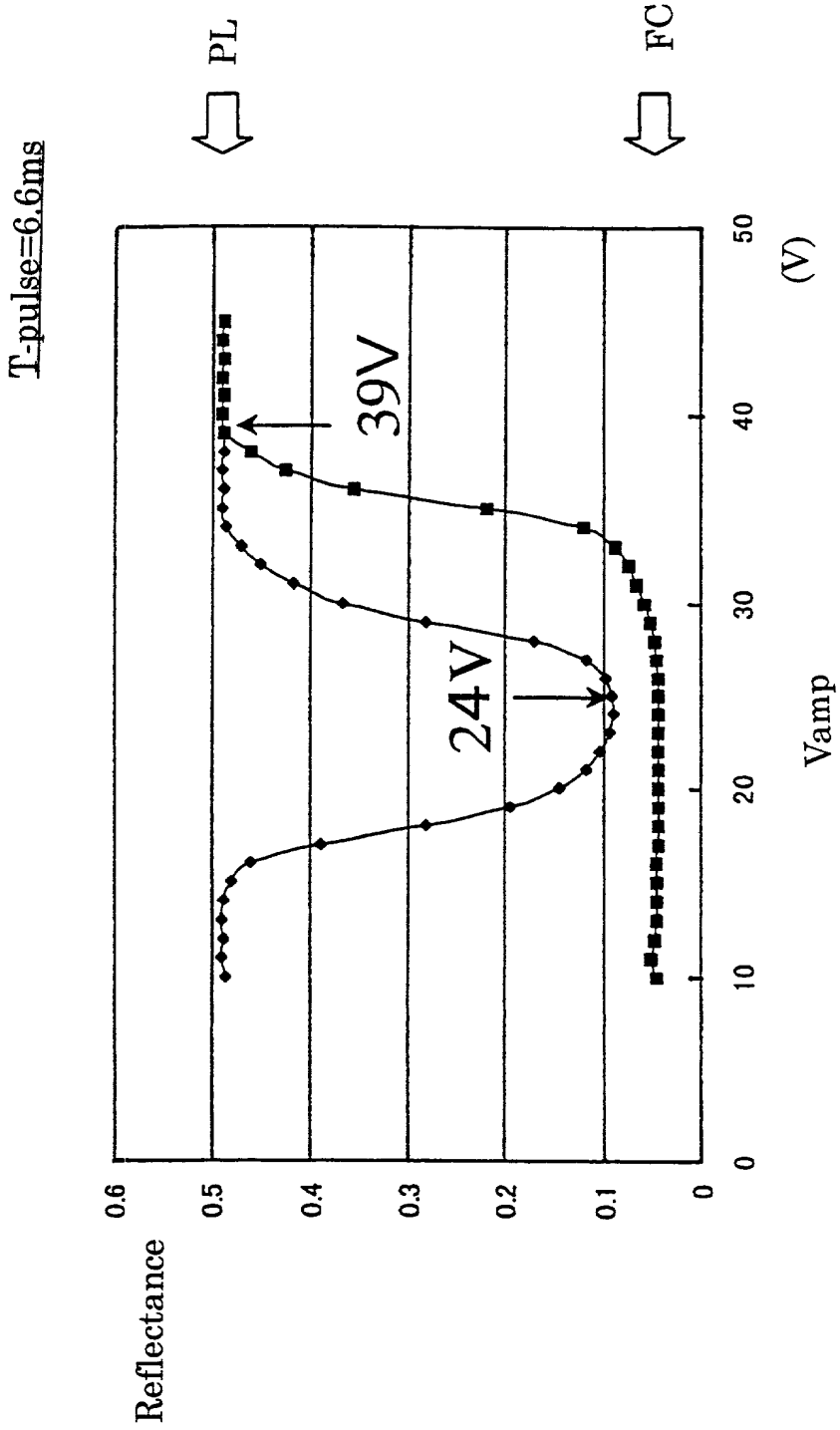

T-pulse=6.6ms
PL
FC
39V
24V
Reflectance
0.6
0.5
0.4
0.3
0.2
0.1
0
0
10
20
30
40
50
(V)
Vamp

Fig. 7

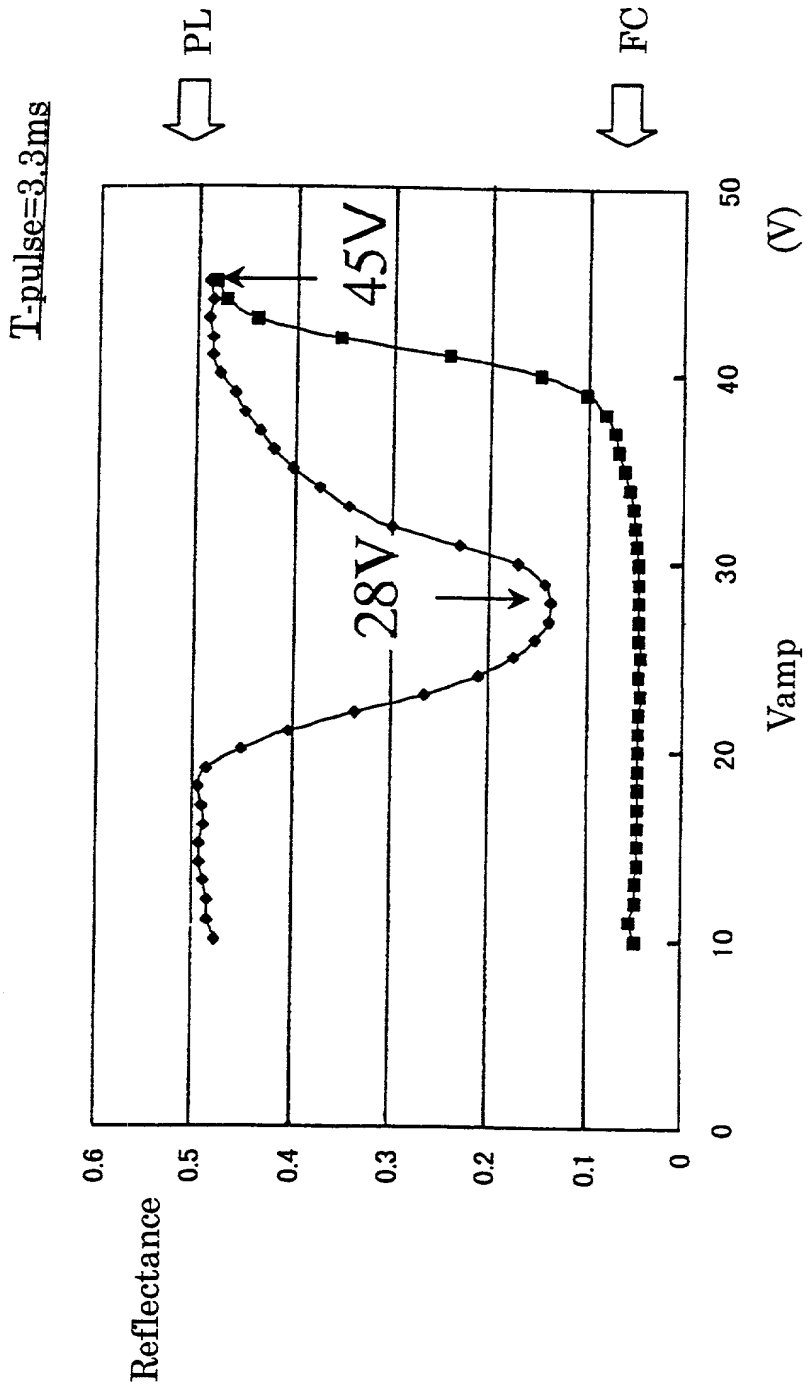

T-pulse=3.3ms
PL
FC
45V
28V
Reflectance
0.6
0.5
0.4
0.3
0.2
0.1
0
0
10
20
30
40
50
Vamp
(V)

Fig. 8

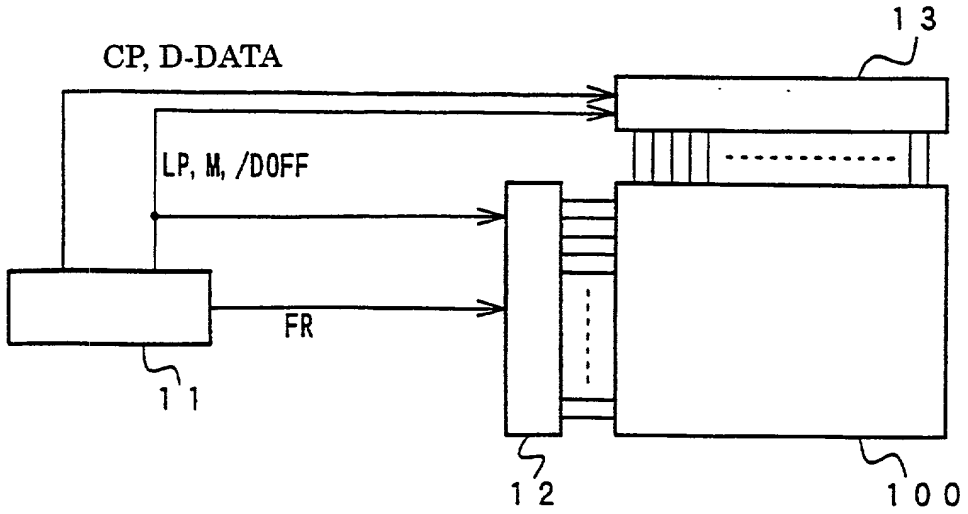

13
CP, D-DATA
LP, M, /DOFF
FR
11
12
100

Fig. 9

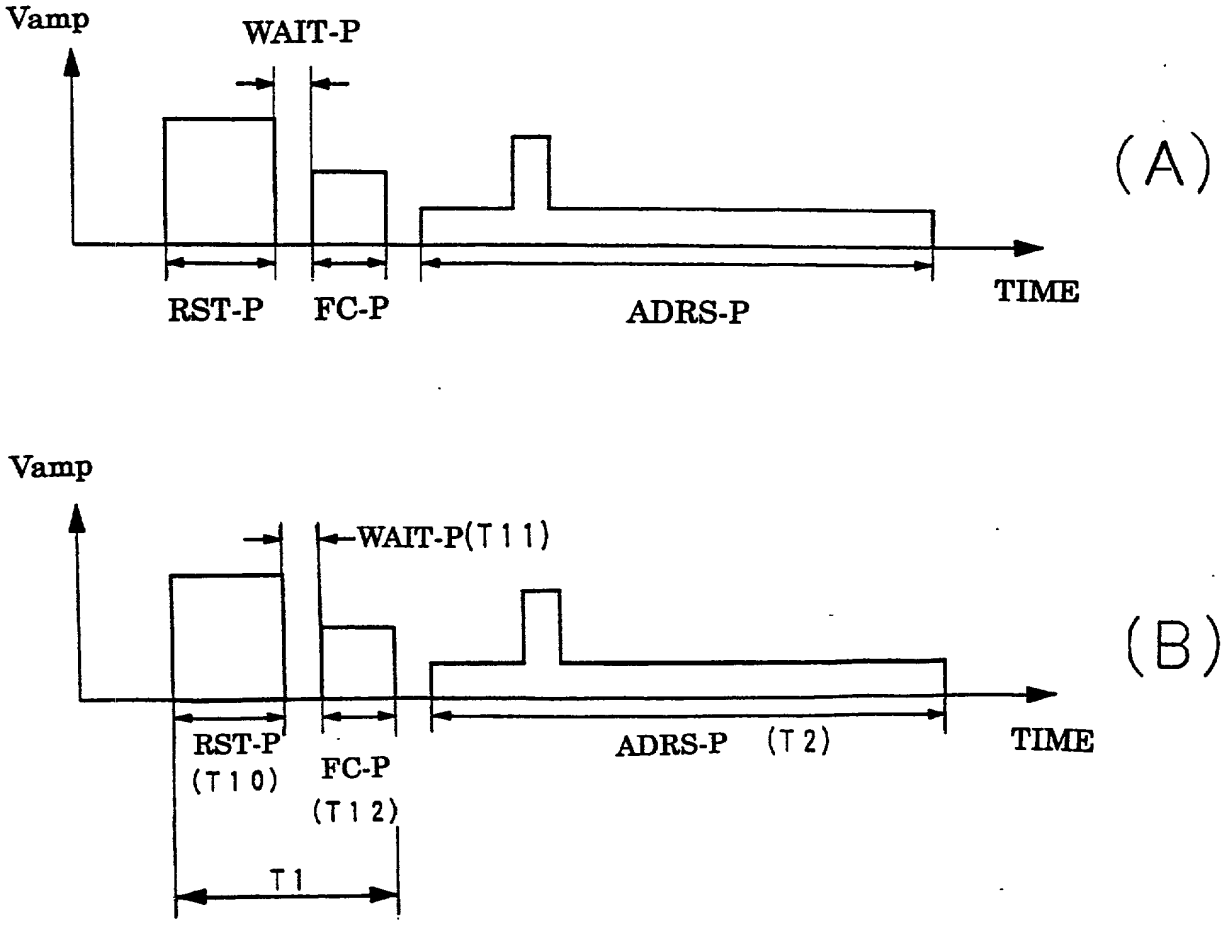

Vamp
WAIT-P
(A)
RST-P
FC-P
ADRS-P
TIME
Vamp
WAIT-P(T11)
(B)
RST-P
(T10)
FC-P
(T12)
T1
ADRS-P (T2)
TIME

Fig. 10

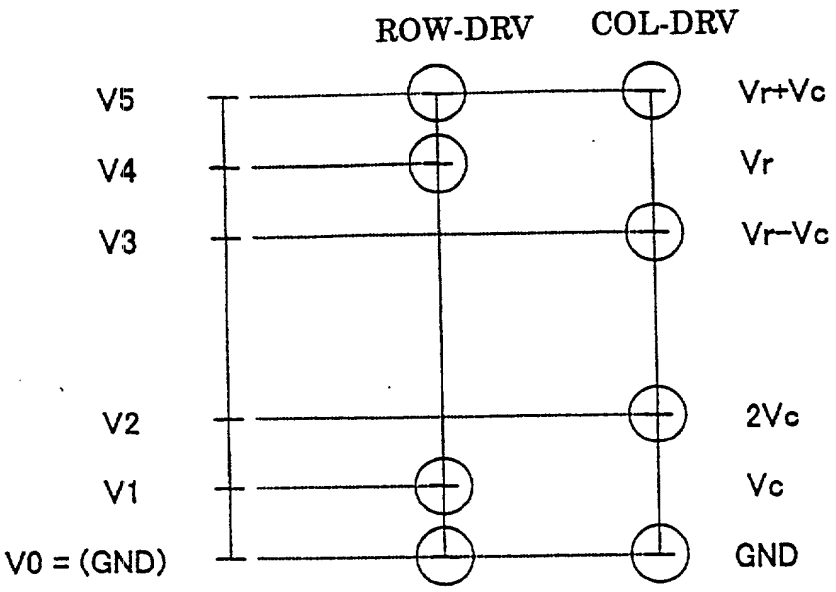


Fig. 11

ROW-DRV

/DOFF	M	SEL/NON-SEL	V-OUT
H	L	SEL	V5
H	H	SEL	V0
H	L	NON-SEL	V1
H	H	NON-SEL	V4
L	X	X	V0

COL-DRV

/DOFF	M	DATA	V-OUT
H	L	H	V0
H	H	H	V5
H	L	L	V2
H	H	L	V3
L	X	X	V0

Fig. 12

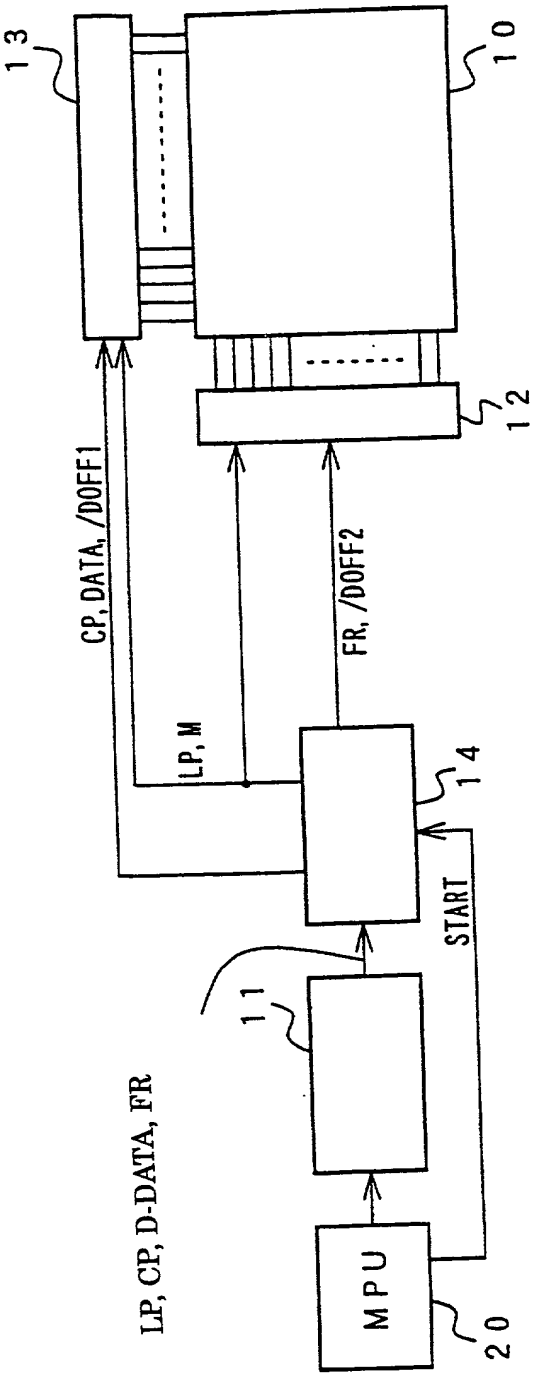

13
10
12
CP, DATA, /DOFF1
LP, M
FR, /DOFF2
14
START
11
LP, CP, D-DATA, FR
MPU
20

Fig. 13

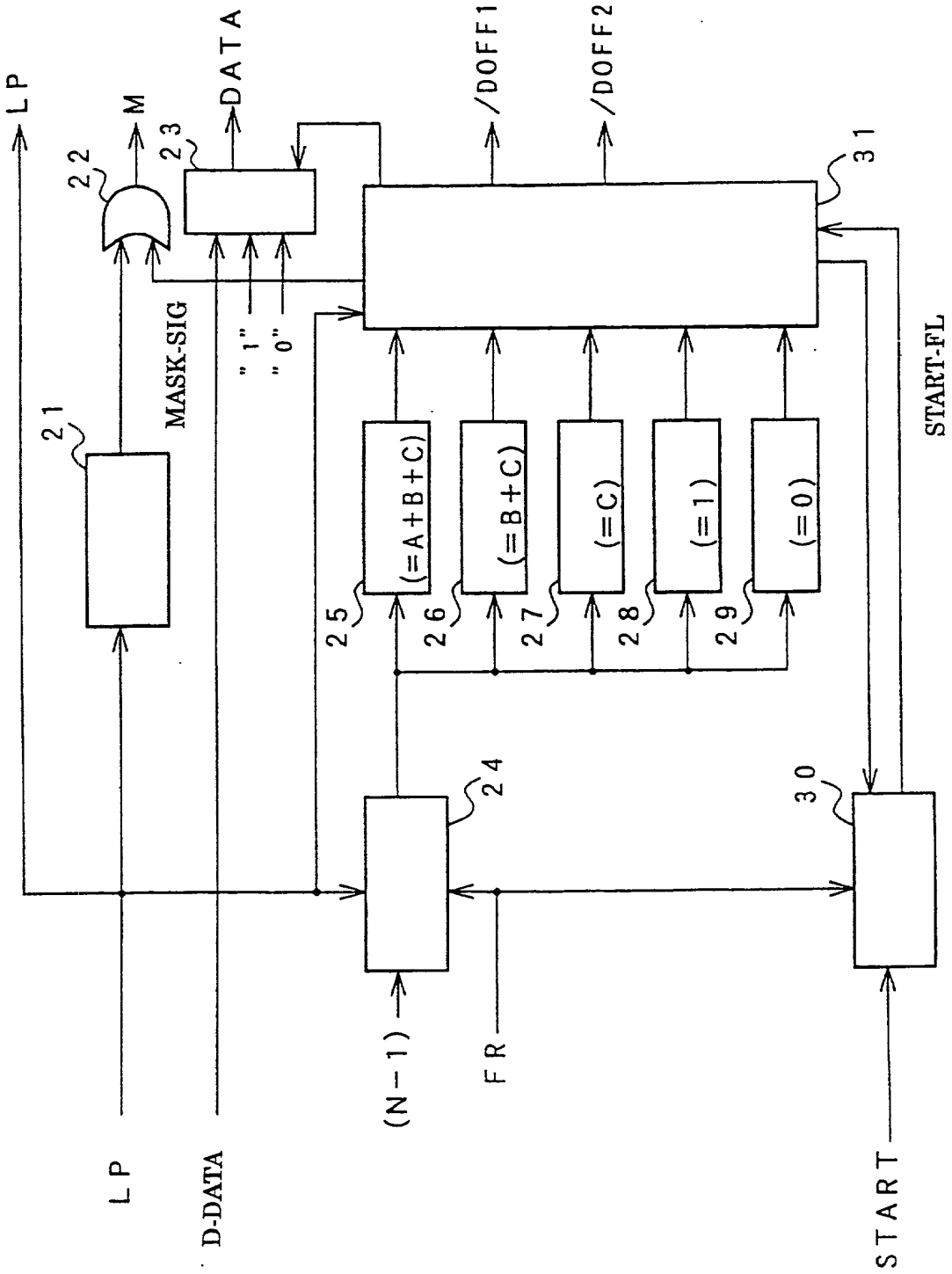

LP
M
DATA
/DOFF1
/DOFF2
22
23
31
MASK-SIG
"1"
"0"
21
(=A+B+C)
(=B+C)
(=C)
(=1)
(=0)
25
26
27
28
29
START-FL
24
30
(N-1)
FR
LP
D-DATA
START

Fig. 14

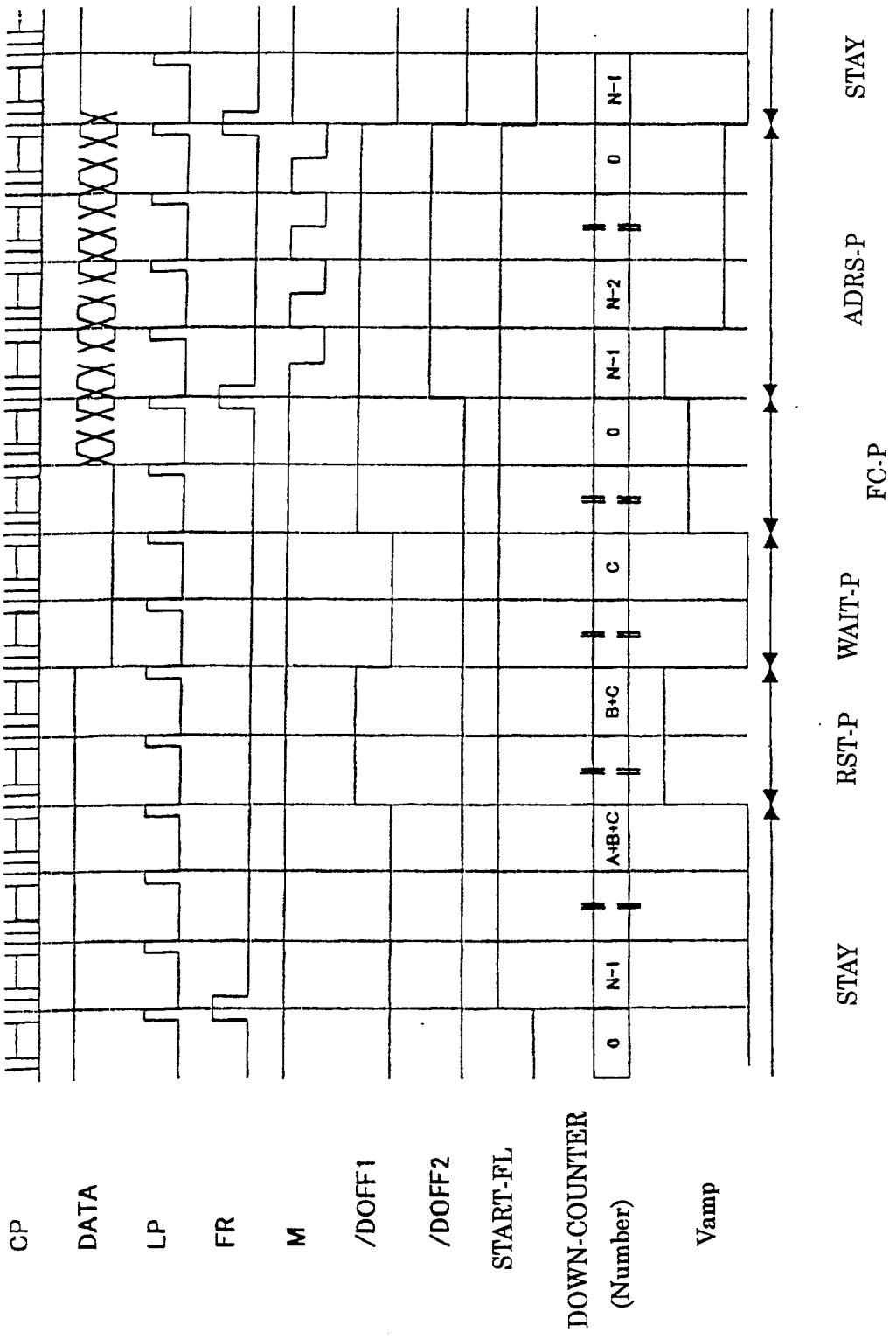

CP
DATA
LP
FR
M
/DOFF1
/DOFF2
START-FL
DOWN-COUNTER
(Number)
Vamp
0
N-1
A+B+C
B+C
C
0
N-1
N-2
0
N-1
STAY
RST-P
WAIT-P
FC-P
ADRS-P
STAY

Fig. 15

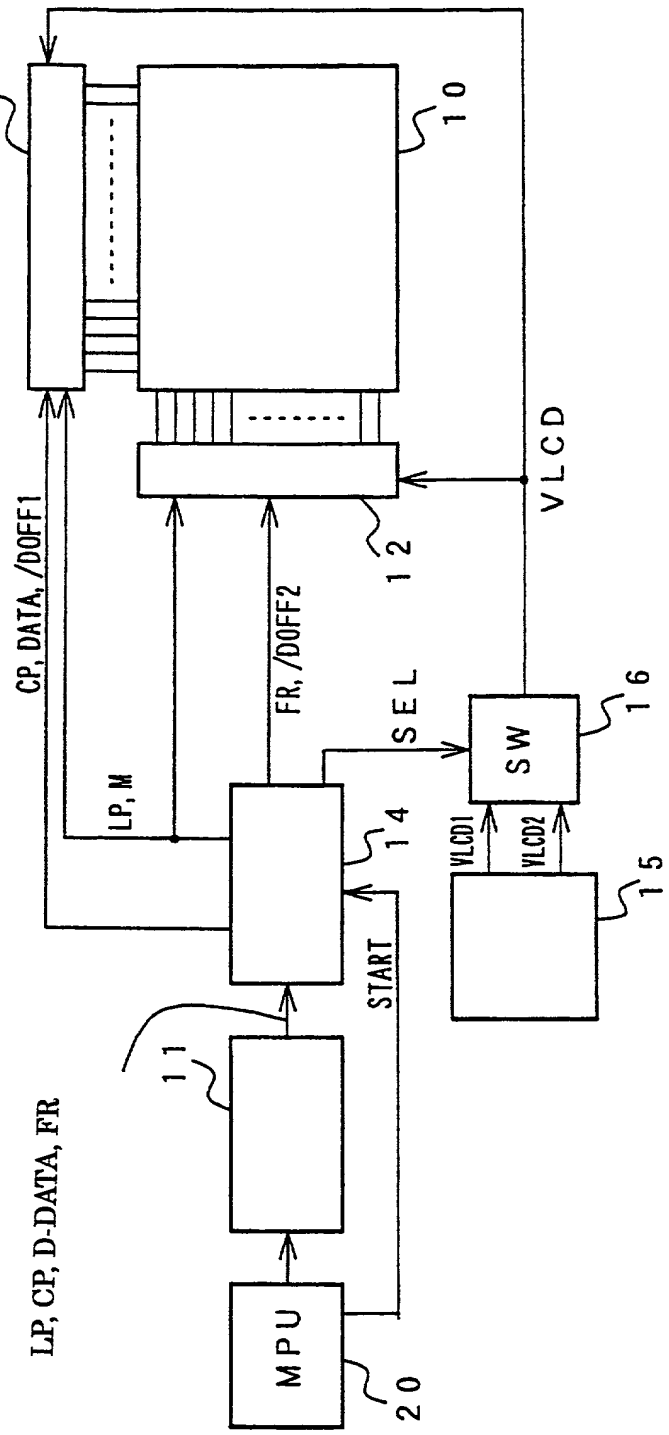

13
10
VLCD
12
CP, DATA, /DOFF1
FR, /DOFF2
SEL
SW
16
LP, M
14
VLCD1
VLCD2
15
START
11
LP, CP, D-DATA, FR
MPU
20

Fig. 16

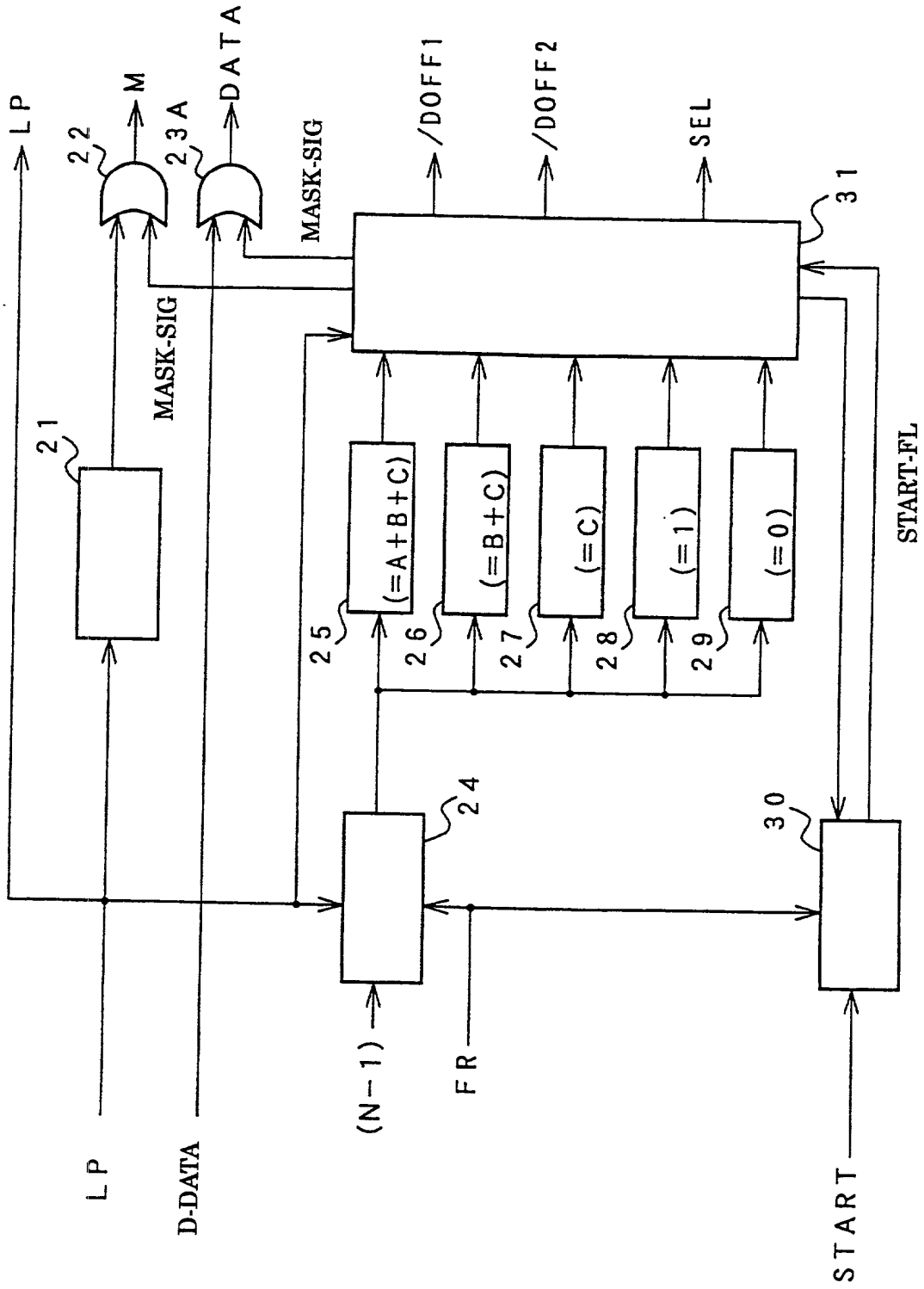

LP
M
DATA
22
23A
MASK-SIG
/DOFF1
/DOFF2
SEL
31
MASK-SIG
21
START-FL
(=A+B+C)
(=B+C)
(=C)
(=1)
(=0)
25
26
27
28
29
24
30
(N-1)
FR
LP
D-DATA
START

Fig. 17

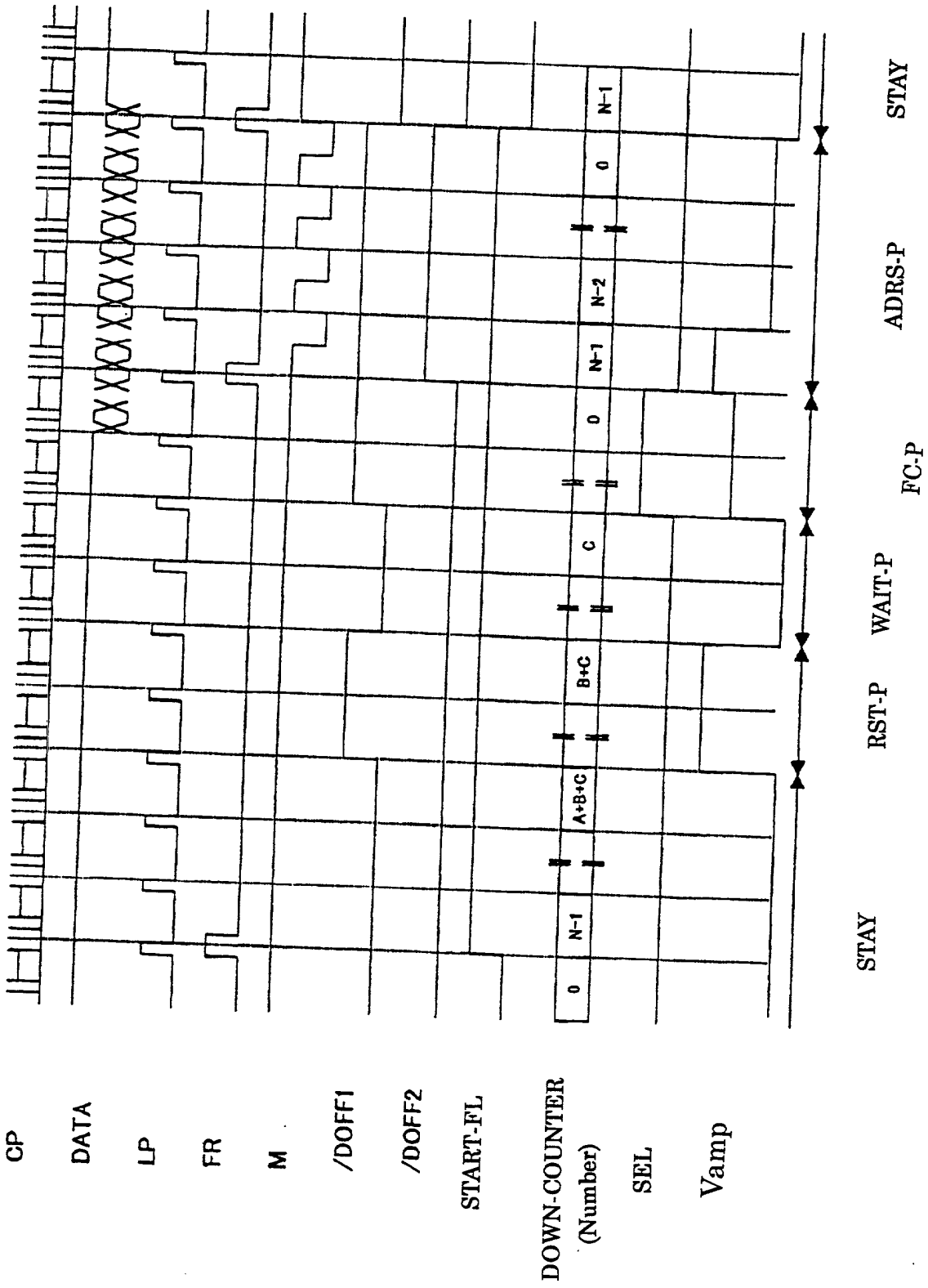

CP
DATA
LP
FR
M
/DOFF1
/DOFF2
START-FL
DOWN-COUNTER (Number)
SEL
Vamp
STAY
RST-P
WAIT-P
FC-P
ADRS-P
STAY
0
N-1
A+B+C
B+C
C
0
N-1
N-2
0
N-1

Fig. 18

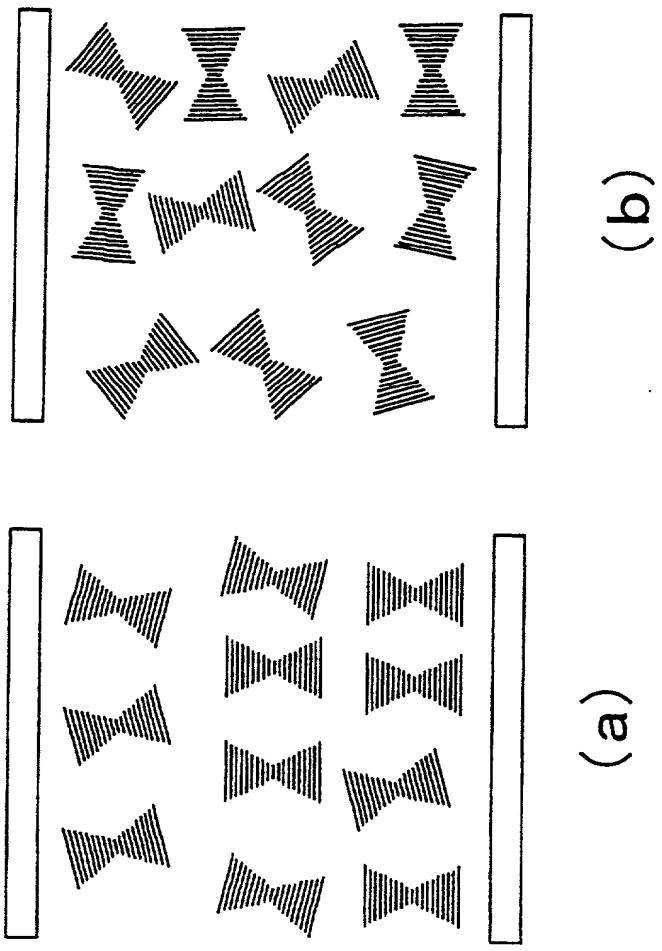


Fig. 19

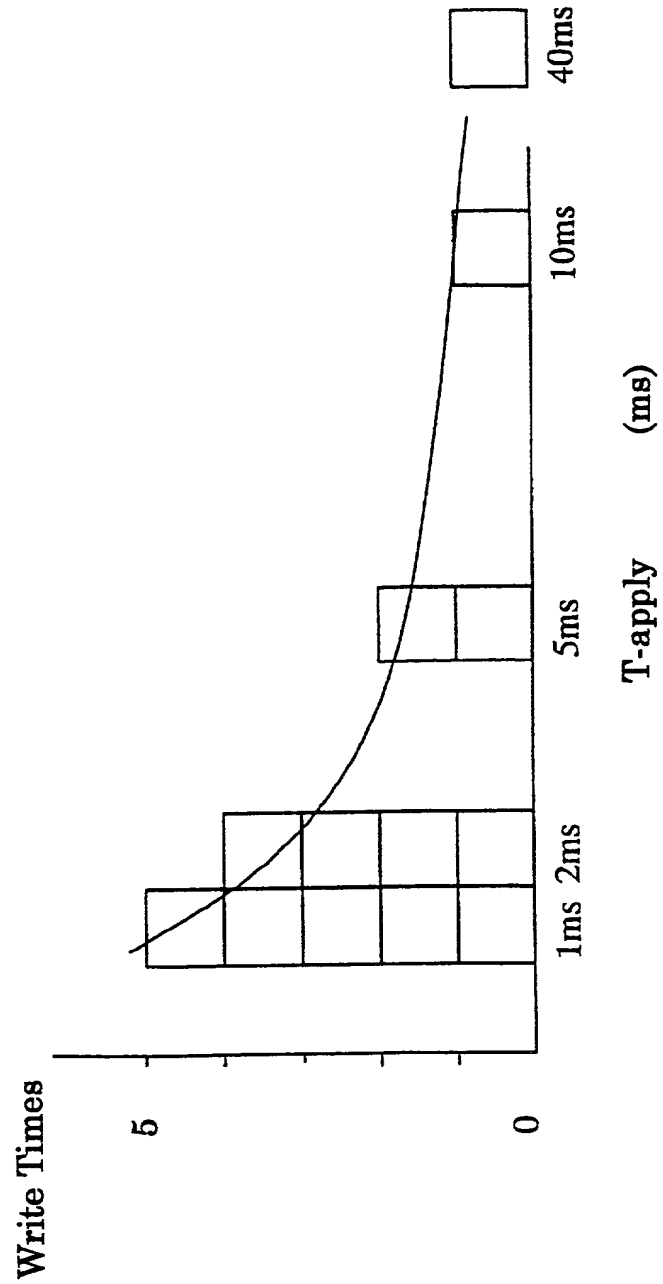

Pulse width and times for establishing a FC state
Write Times
5
0
1ms
2ms
5ms
10ms
40ms
T-apply (ms)

Fig. 20

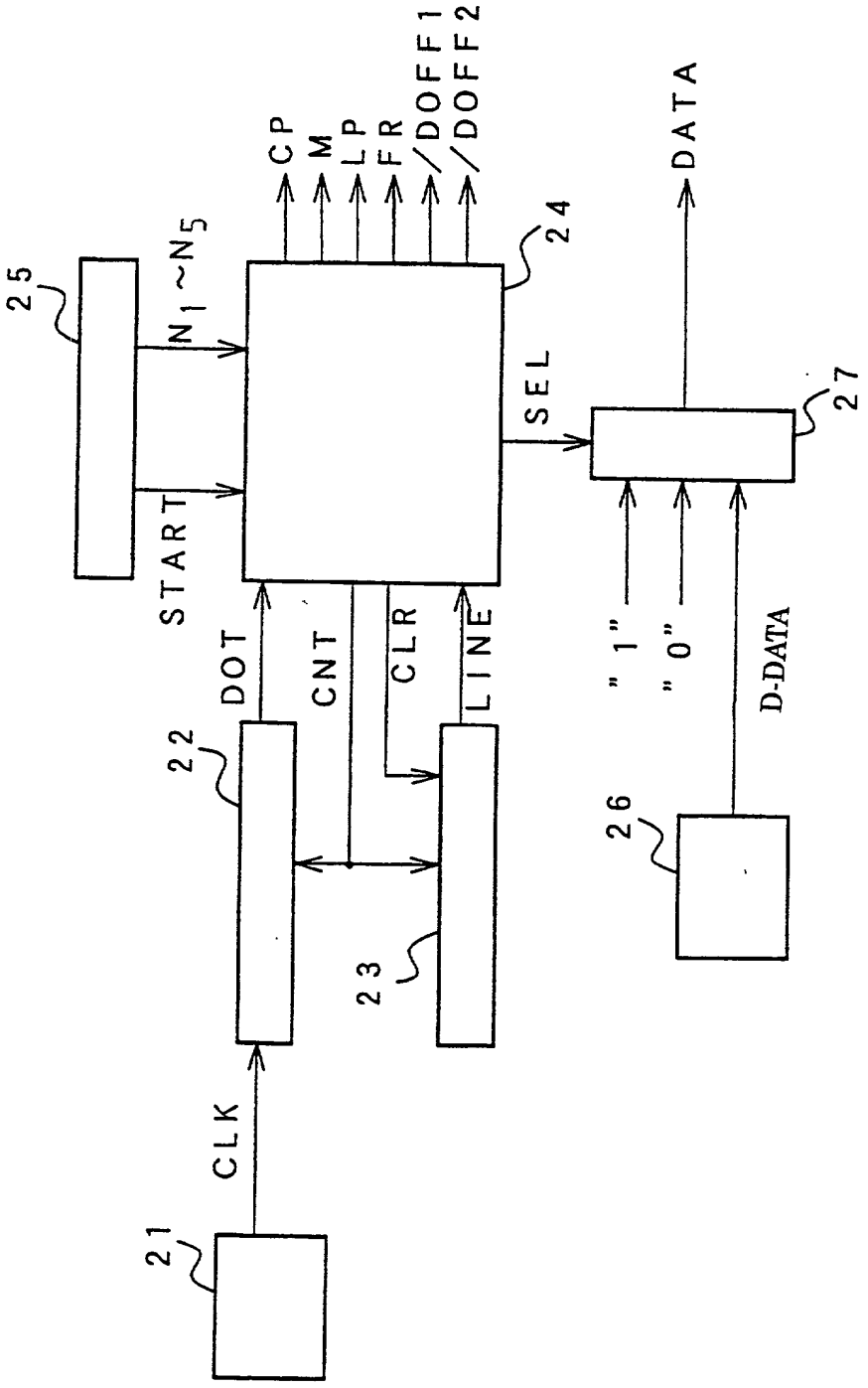

CP
M
LP
FR
DOFF1
DOFF2
DATA
24
25
N1~N5
SEL
27
START
DOT
CNT
CLR
LINE
" 1"
" 0"
D-DATA
22
23
26
CLK
21

Fig. 21

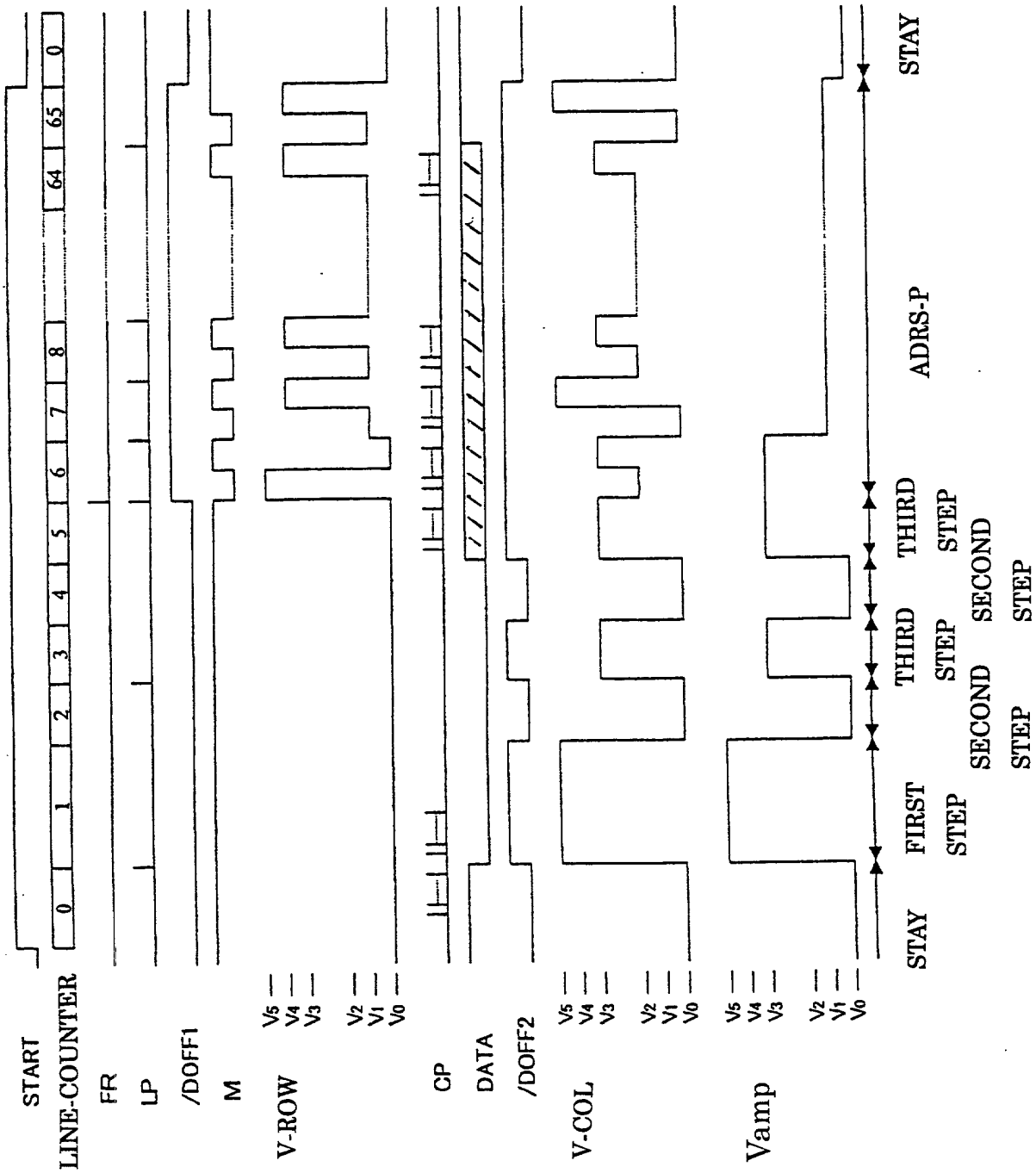

START
LINE-COUNTER
0
1
2
3
4
5
6
7
8
64
65
0
FR
LP
/DOFF1
M
V-ROW
V5
V4
V3
V2
V1
V0
CP
DATA
/DOFF2
V-COL
Vamp
STAY
FIRST
STEP
SECOND
STEP
THIRD
STEP
SECOND
STEP
THIRD
STEP
ADRS-P
STAY

Fig. 22

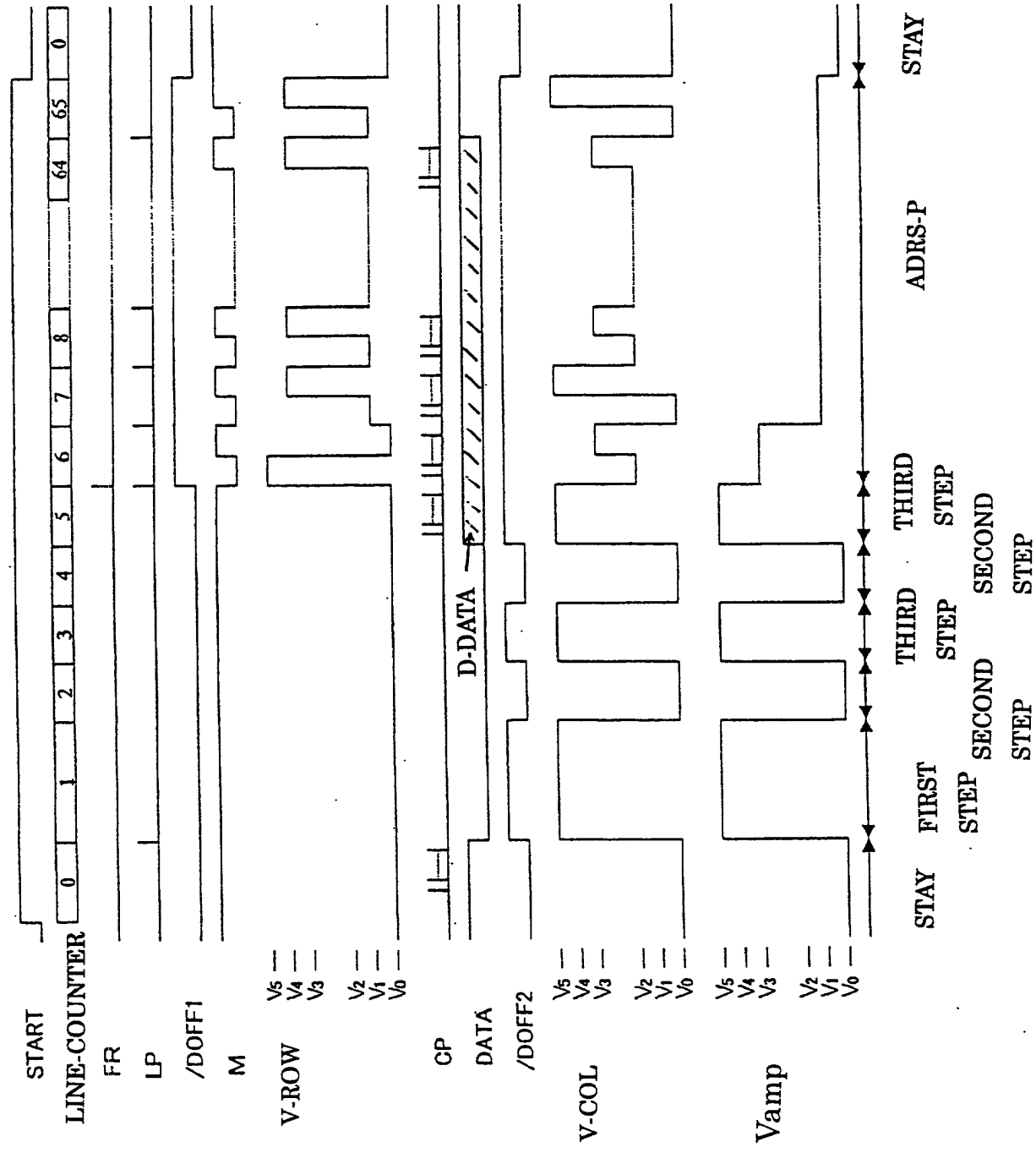

START
LINE-COUNTER
0
1
2
3
4
5
6
7
8
64
65
0
FR
LP
/DOFF1
M
V-ROW
V5
V4
V3
V2
V1
V0
CP
DATA
D-DATA
/DOFF2
V-COL
Vamp
STAY
FIRST STEP
SECOND STEP
THIRD STEP
SECOND STEP
THIRD STEP
ADRS-P
STAY

Fig. 23

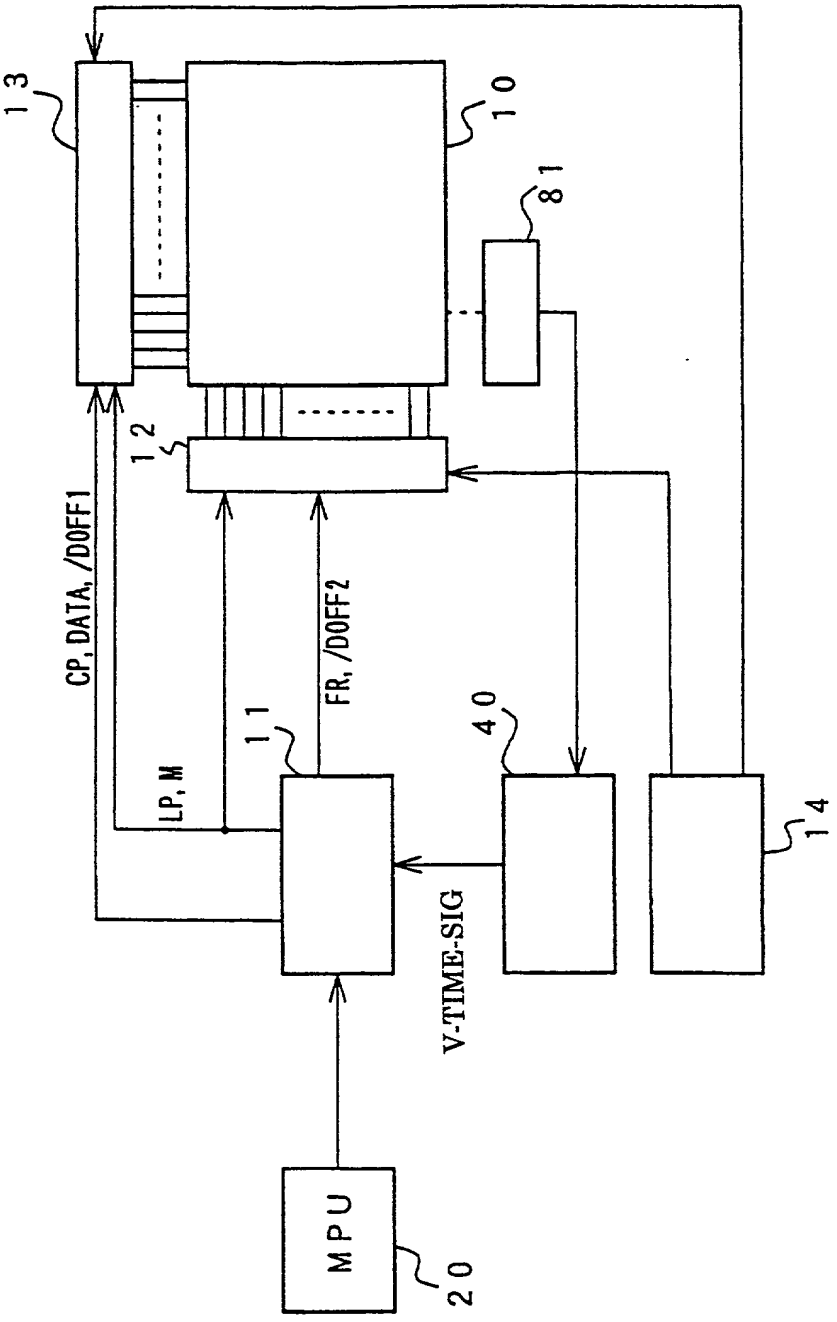


Fig. 24

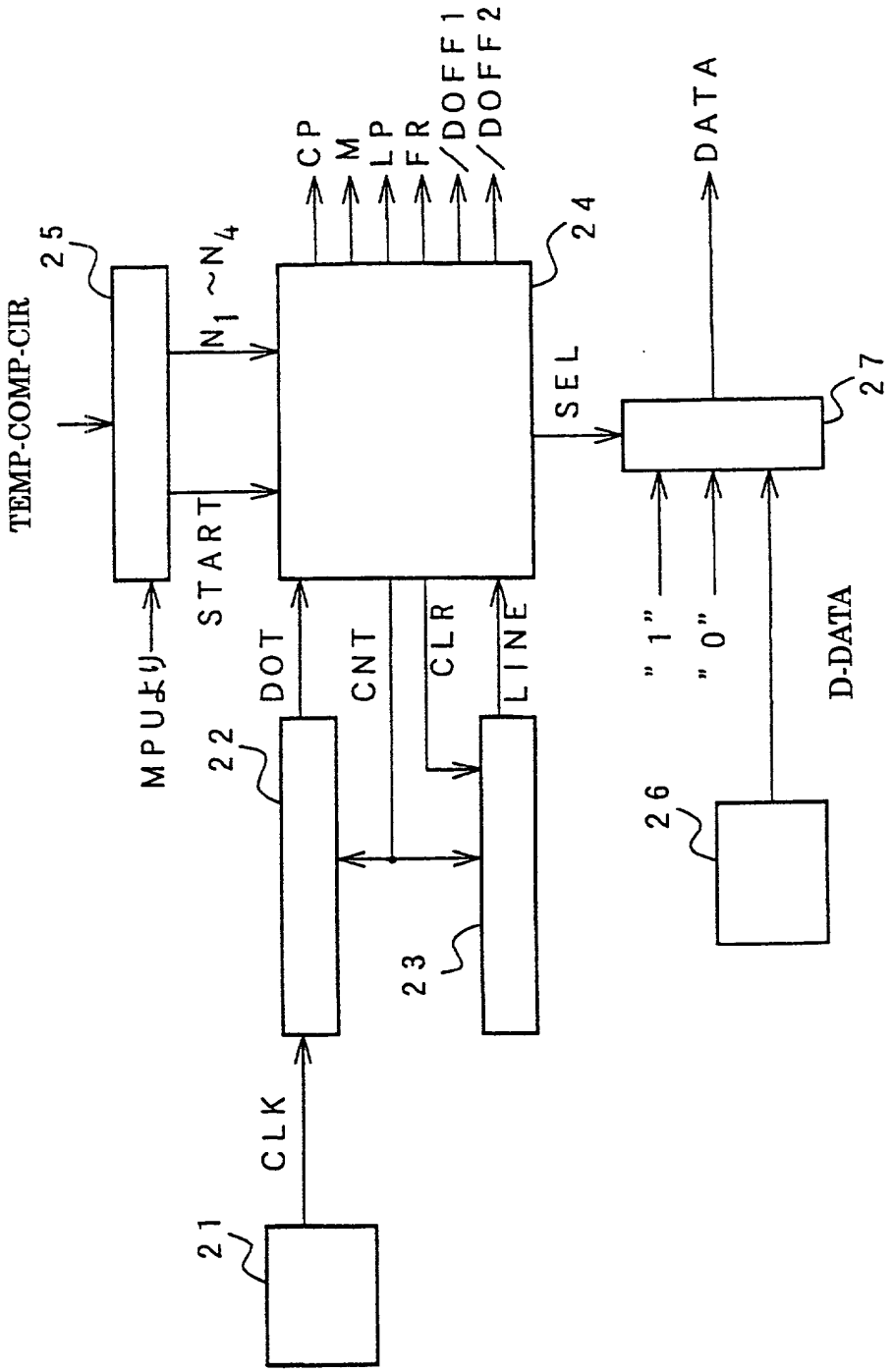

TEMP-COMP-CIR
25
$N_1 \sim N_4$
START
MPUより
DOT
CNT
CLR
LINE
22
23
24
CP
M
LP
FR
DOFF1
DOFF2
SEL
DATA
27
" 1"
" 0"
D-DATA
26
CLK
21

Fig. 25

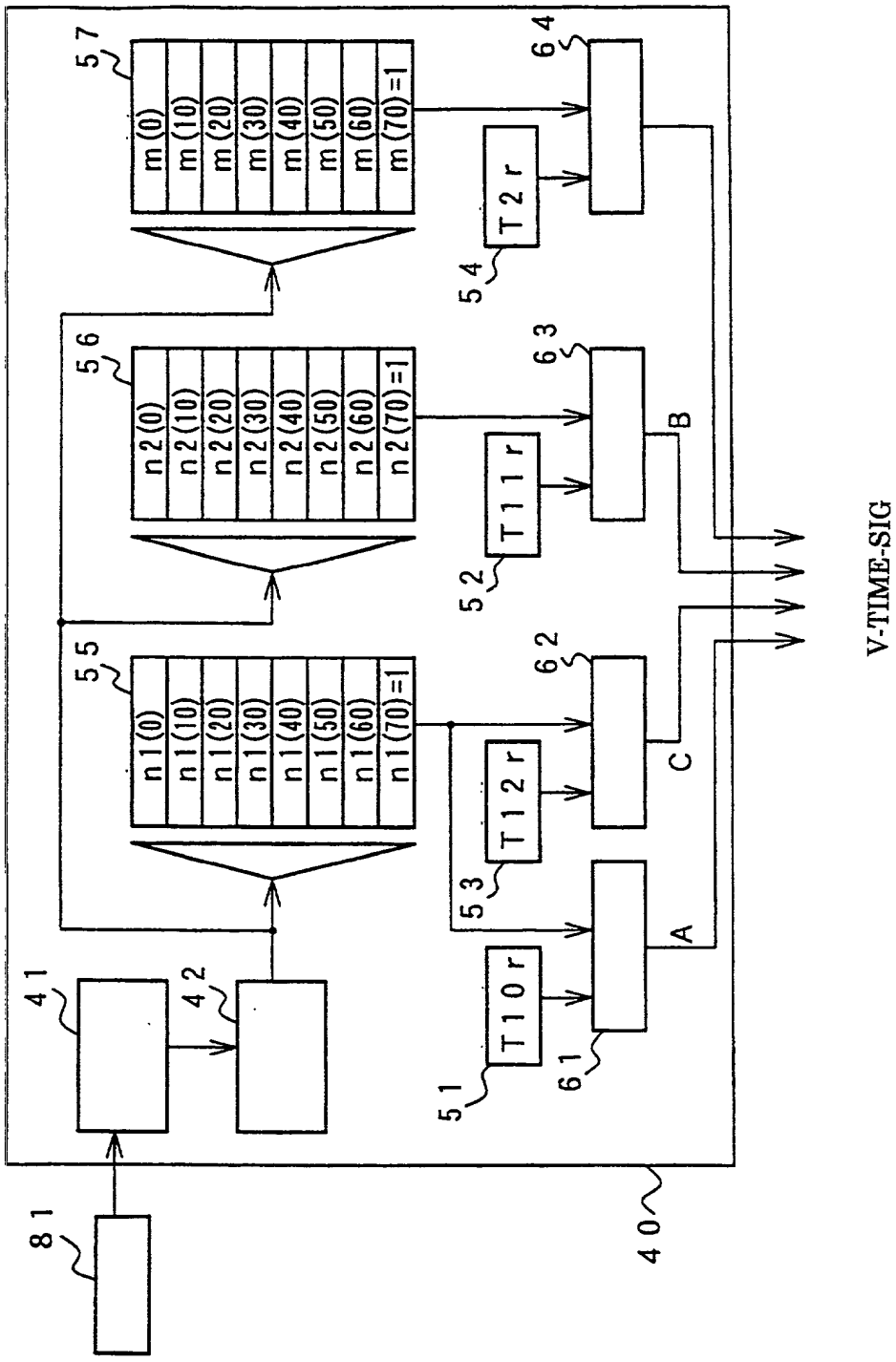

57
m(0)
m(10)
m(20)
m(30)
m(40)
m(50)
m(60)
m(70)=1
64
T2r
54
56
n2(0)
n2(10)
n2(20)
n2(30)
n2(40)
n2(50)
n2(60)
n2(70)=1
63
T11r
52
B
55
n1(0)
n1(10)
n1(20)
n1(30)
n1(40)
n1(50)
n1(60)
n1(70)=1
62
T12r
53
C
A
T10r
51
61
41
42
81
40
V-TIME-SIG

Fig. 26

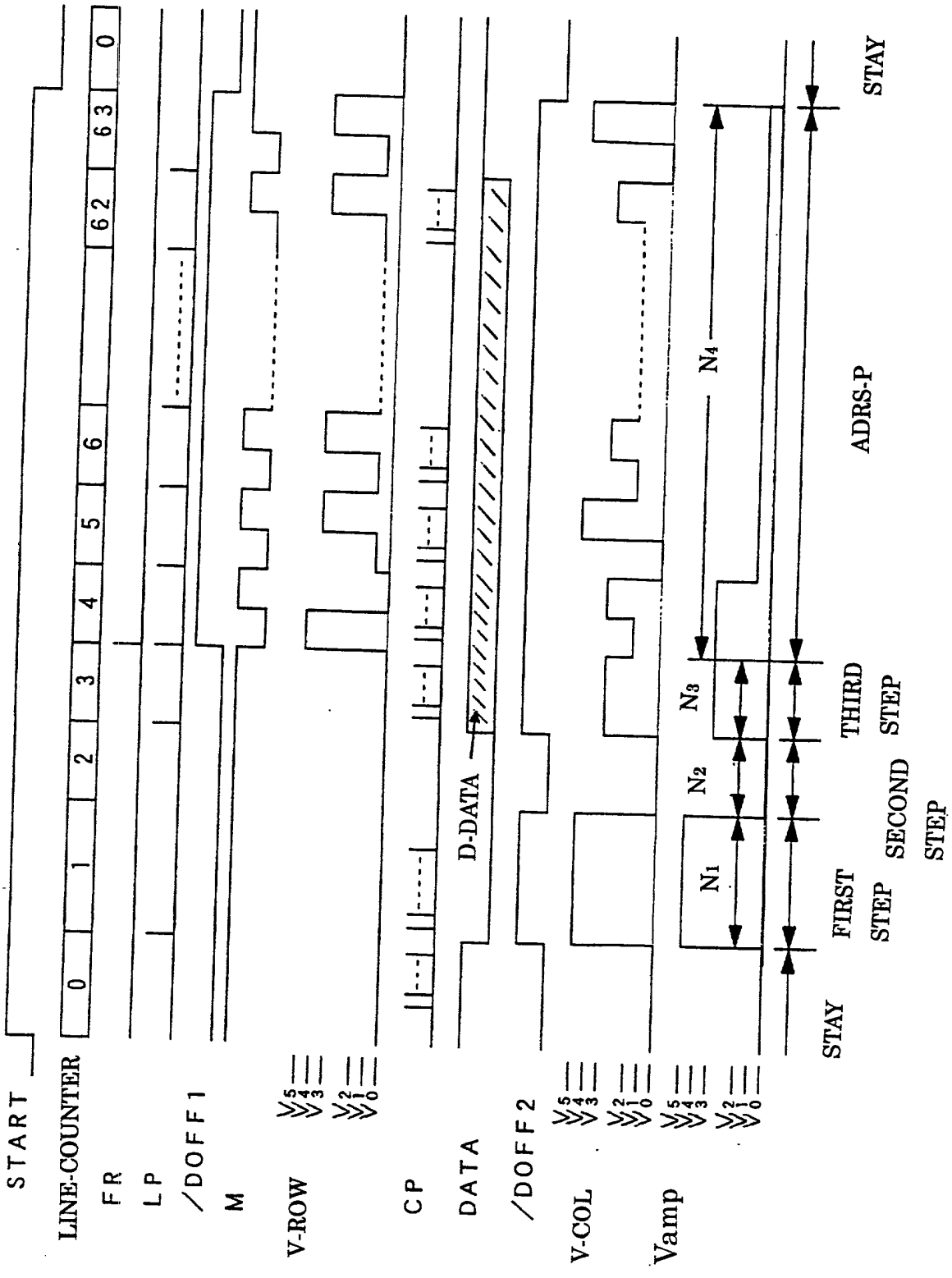

START
LINE-COUNTER
0
1
2
3
4
5
6
62
63
0
FR
LP
/DOFF1
M
V-ROW
CP
DATA
D-DATA
/DOFF2
V-COL
Vamp
N1
N2
N3
N4
STAY
FIRST STEP
SECOND STEP
THIRD STEP
ADRS-P
STAY

Fig. 27

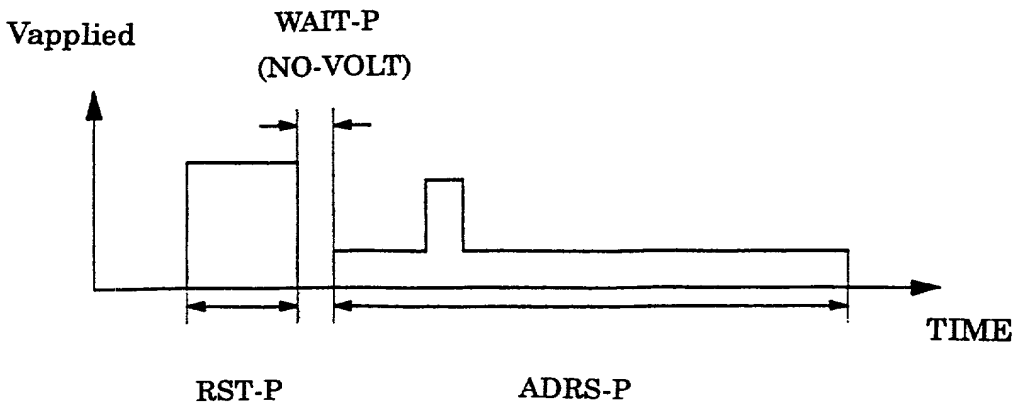


Fig. 28

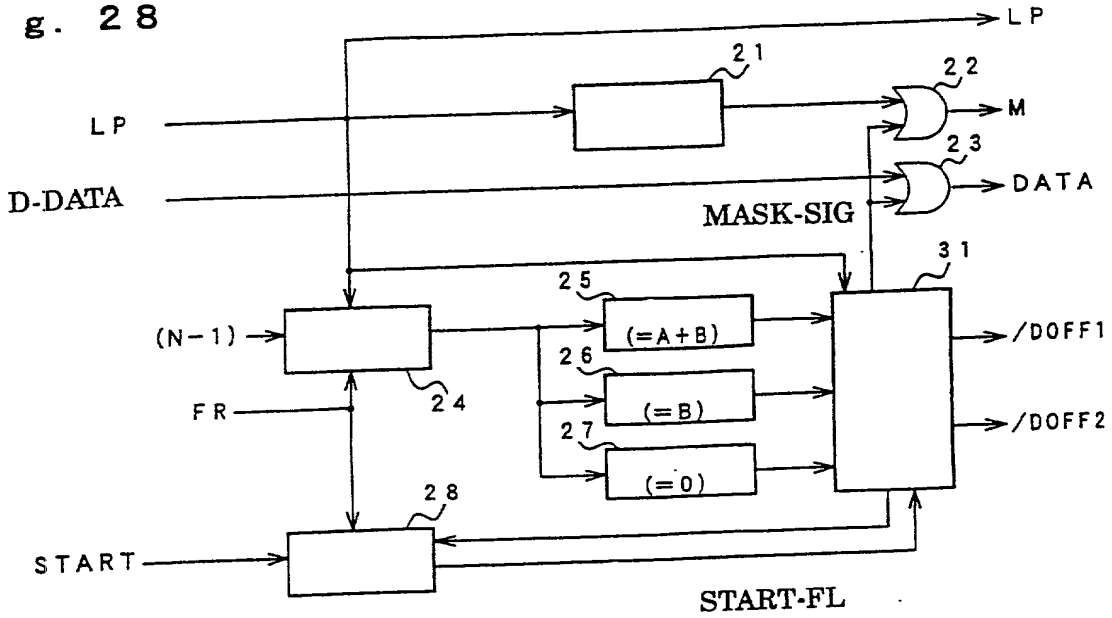

LP
21
22
M
LP
23
DATA
D-DATA
MASK-SIG
31
25
(N-1)
(=A+B)
/DOFF1
26
(=B)
24
FR
/DOFF2
27
(=0)
28
START
START-FL

Fig. 29

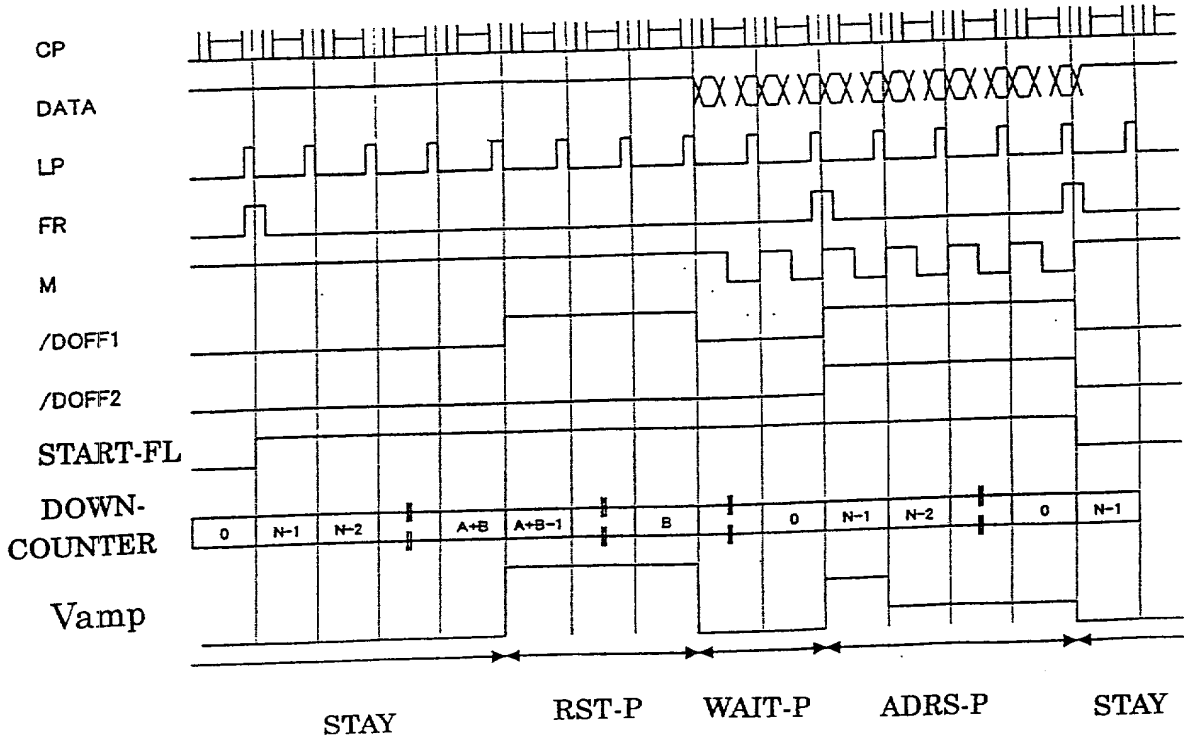

CP
DATA
LP
FR
M
/DOFF1
/DOFF2
START-FL
DOWN-COUNTER
0
N-1
N-2
A+B
A+B-1
B
0
N-1
N-2
0
N-1
Vamp
STAY
RST-P
WAIT-P
ADRS-P
STAY

Fig. 30

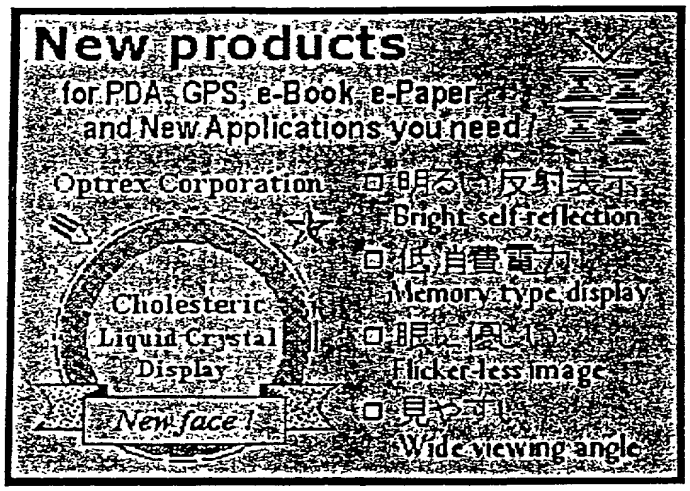

New products
for PDA, GPS, e-Book, e-Paper
and New Applications you need!
Optrex Corporation
Cholesteric
Liquid Crystal
Display
New face!
Bright self-reflection
Memory type display
Flicker-less image
Wide viewing angle

Fig. 31